2-CHANNEL ULTRA-LOW CLAMP VOLTAGE ESD SOLUTION WITH SERIES-RESISTOR ISOLATION

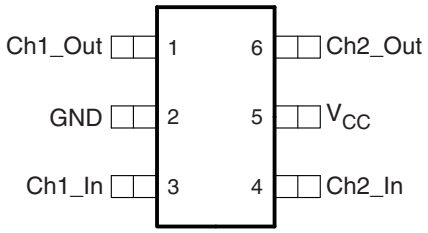
FEATURES

- **Ultra-Low Clamp Voltage Ensures the Protection of Ultra-Low Voltage Core Chipset During ESD Events**
- **Exceeds ESD Protection to IEC61000-4-2 (Level 4)**
- **Matching of Series Resistor (R =1 Ω) of ±8 mΩ (Typical)**
- **Differential Channel Input Capacitance Matching of 0.02 pF (Typical)**
- **High-Speed Data Rate and EMI Filter Action at High Frequencies (–3 dB Bandwidth, ≈3 GHz)**
- **Available in 6-Pin Small-Outline Transistor [SOT (DBV)] Package**
- **Flow-Through Single-In-Line Pin Mapping for the High-Speed Lines Ensures no Additional Board Layout Burden While Placing the ESD Protection Chip Near the Connector**

APPLICATIONS

- **Hi-Speed USB**
- **IEEE 1394 Interface**
- **Low-Voltage Differential Signaling (LVDS)**
- **Mobile Display Digital Interface (MDDI)/Mobile Industry Processor Interface (MIPI)**
- **HS Signal**

DBV PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TPD2S017 provides a robust system-level ESD solution for the high-speed lines interfacing low-voltage, ESD-sensitive core chipset. This device offers two stage ESD clamps in each line with ≈1-Ω series resistor isolation. This architecture allows the device to generate very low clamp voltage during system level ESD strikes. Due to the series resistor component, the TPD2S017 provides a controlled filter roll-off for even greater spurious EMI suppression and signal integrity. This device offers a flow-through pin mapping for ease of board layout. The monolithic silicon technology allows matching component values, including clamp capacitance, series resistor matching, etc., between the differential signal pairs. Tight matching of the line capacitance and series resistors ensure that the differential signal distortion due to added ESD clamp remains minimal, and also allow the part to operate at high-speed differential data rate (in excess of 1.5 Gbps).

The TPD2S017 confirms the IEC61000-4-2 (Level 4) ESD protection and ±15 kV HBM ESD protection. This device is offered in space saving DBV packages.

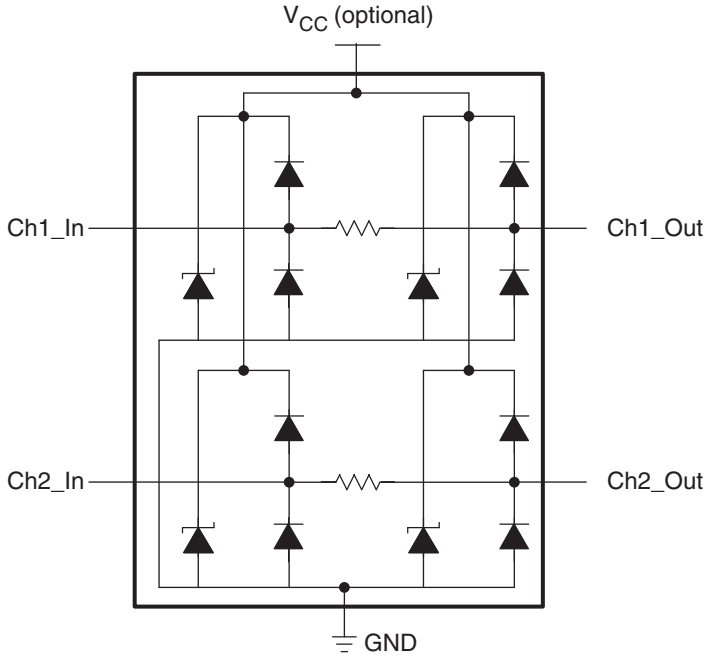
The TPD2S017 is characterized for operation over ambient air temperature of –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	TPD2S017DBVR	NFTF

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

CIRCUIT DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Ch1_In Ch2_In	3 4	I	High-speed ESD clamp input
Ch1_Out Ch2_Out	1 6	O	High-speed ESD clamp output
GND	2	–	Ground
V_{CC}	5	–	Optional power

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	IO voltage range	0	5	V
T_{stg}	Storage temperature range	–85	125	°C
TA	Operating temperature	–40	85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD RATINGS

PARAMETER		MIN	MAX	UNIT
IEC 61000-4-2 Contact Discharge	Out pin		±11	kV
	In pin		±11	
Human Body Model	In and out pins		±15	kV

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A \le 25°C$	$T_A = 70°C$ POWER RATING
DBV	463.18 mW	-4.63 mW/C	254.75 mW

(1) Derating factor is defined as the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Series resistor			1		Ω
I_{IO}	Current from I/O pins	V_{IO} = 3 V		0.01	0.1	µA
ΔRS	Channel-to-channel resistance match	V_{IO} = 3 V		±8	±15	mΩ
V_D	Diode forward voltage for lower clamp	I_D = 8 mA	–0.6	–0.8	–0.95	V
R_{DYN}	Dynamic resistance (for I/O clamp)	I = 9A		0.8		Ω
C_{IO}	IO capacitance	V_{IO} = 2.5 V		1		pF
V_{BR}	Break-down voltage	I_O = 1 mA	11	12		V

TYPICAL CHARACTERISTICS

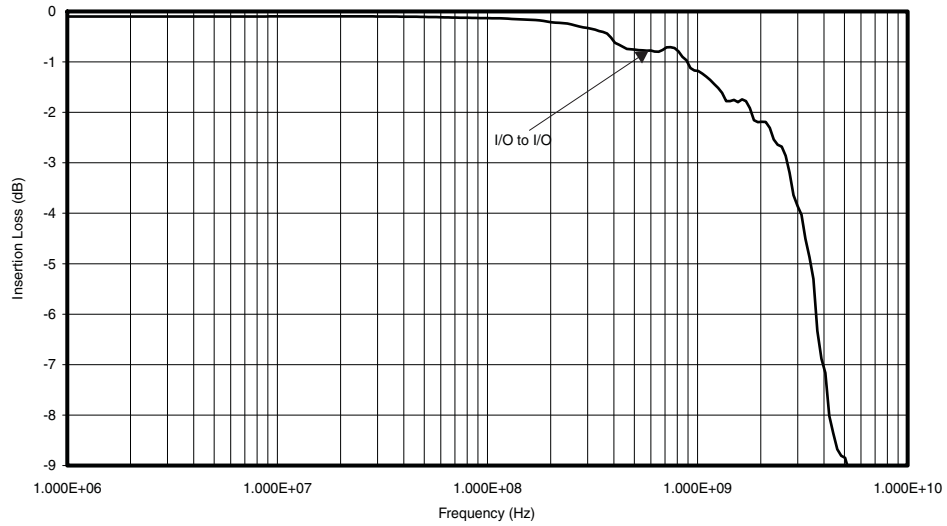


Figure 1. Insertion Loss Data (S21)

TYPICAL CHARACTERISTICS (continued)

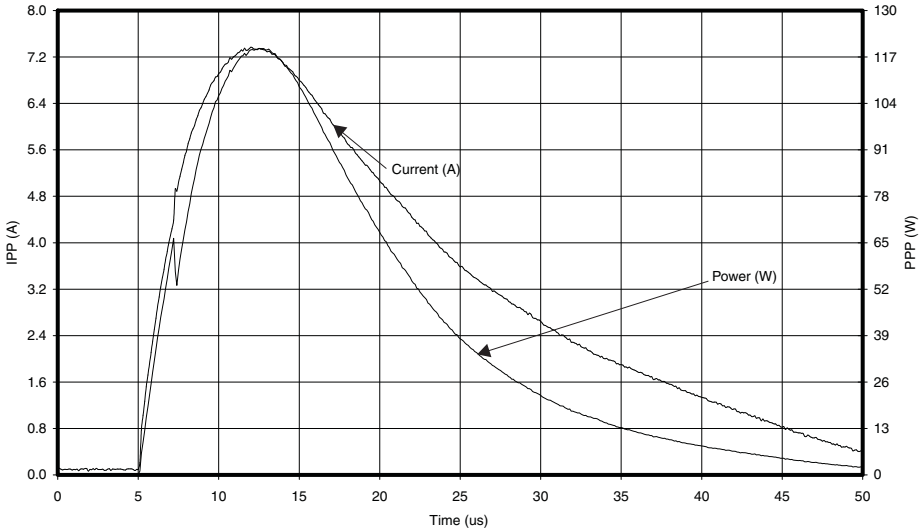


Figure 2. Peak Pulse Waveforms
Ch1_Out, PUT wrt GND, V_{CC} = 5.0 V

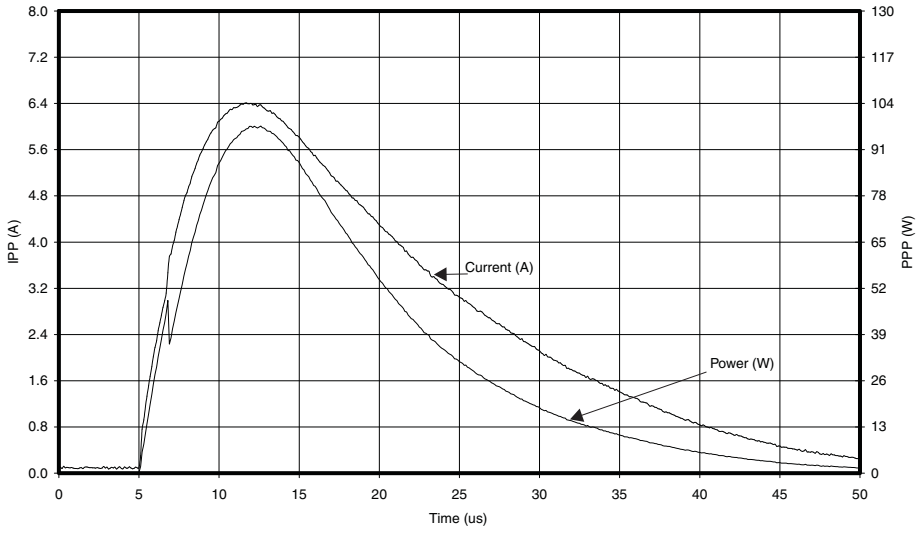


Figure 3. Peak Pulse Waveforms
Ch2_In, PUT wrt GND, V_{CC} = 5.0 V

TYPICAL CHARACTERISTICS (continued)

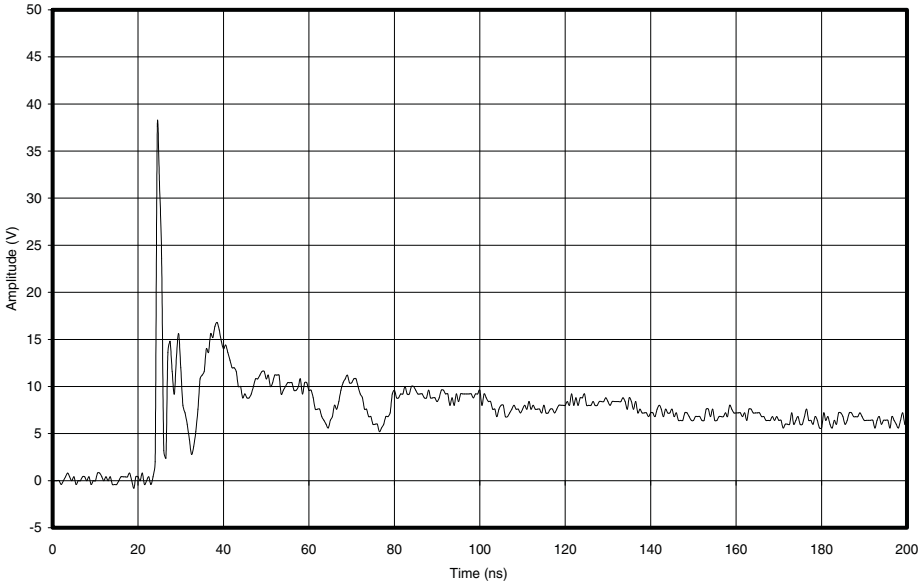


Figure 4. IEC Clamping Waveforms
8 kV Contact, 1 GHz Bandwidth

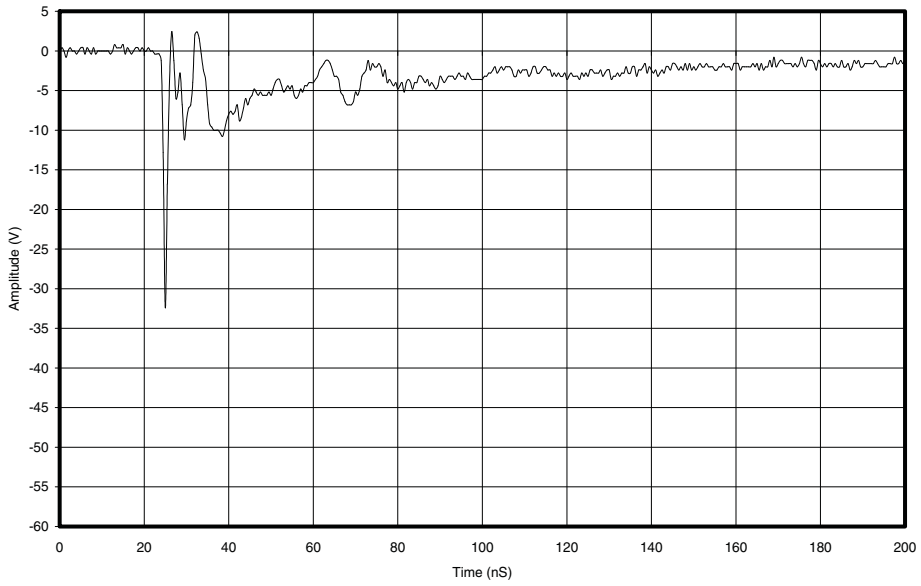


Figure 5. IEC Clamping Waveforms
–8 kV Contact, 1 GHz Bandwidth

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2S017DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	NFT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

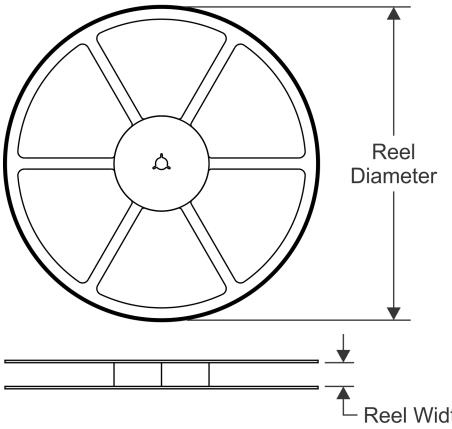
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

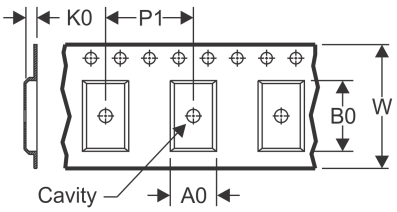
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

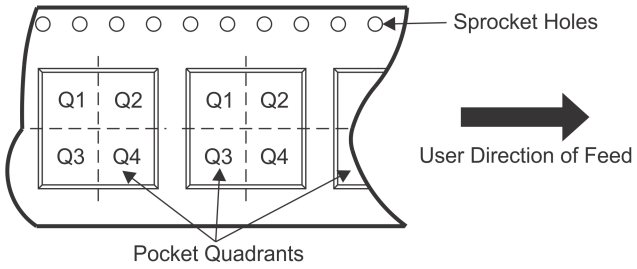


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

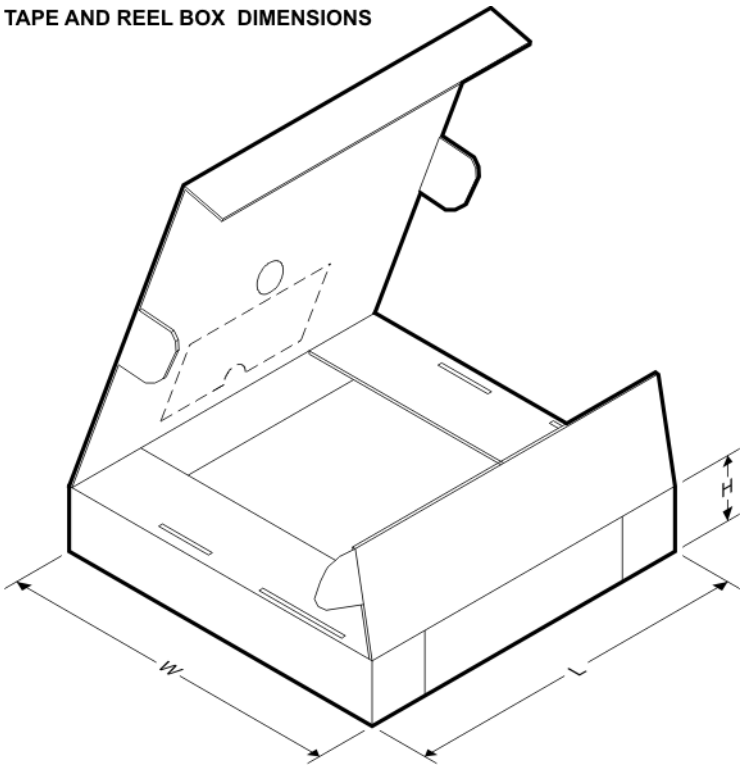
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2S017DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

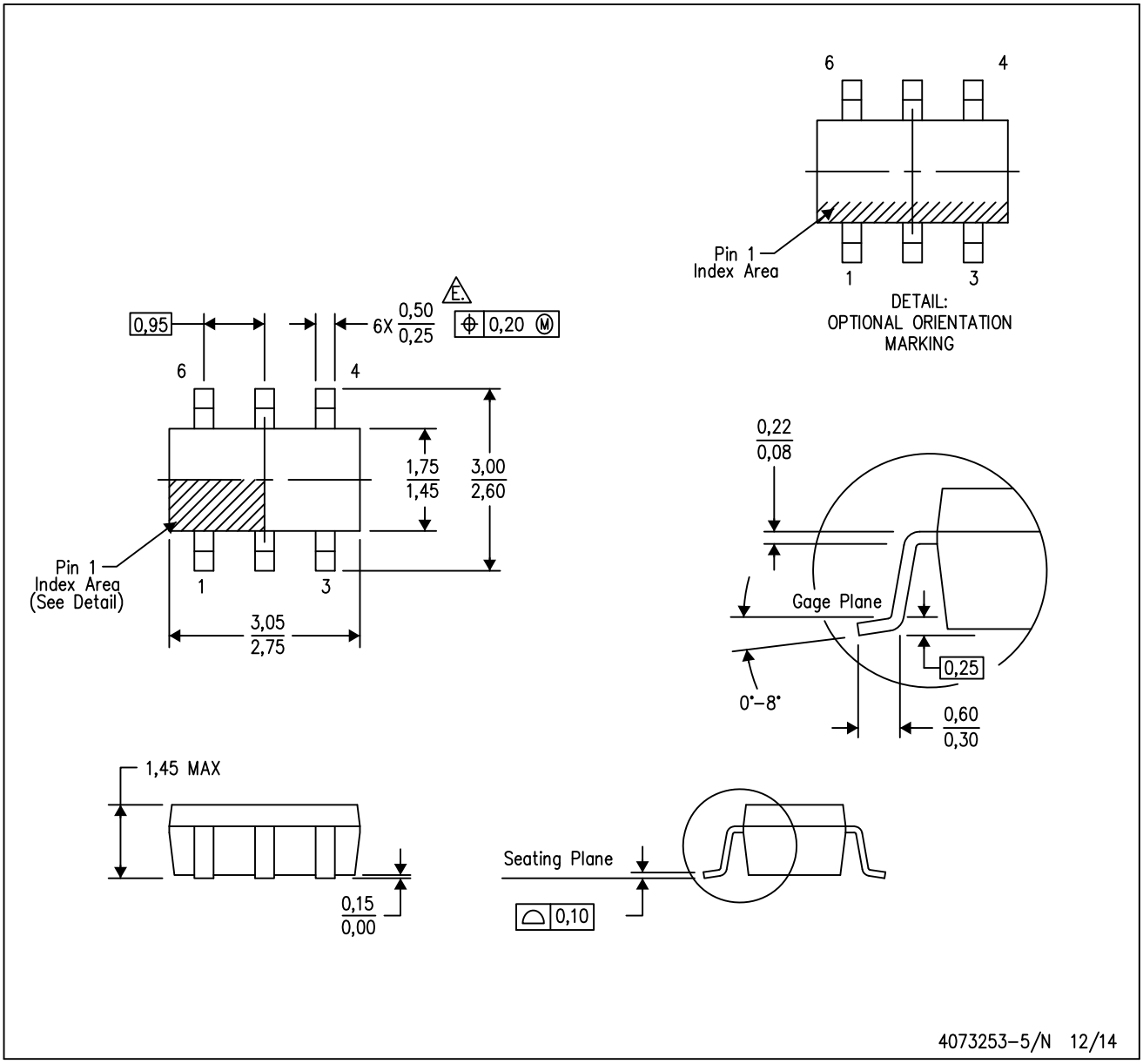
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

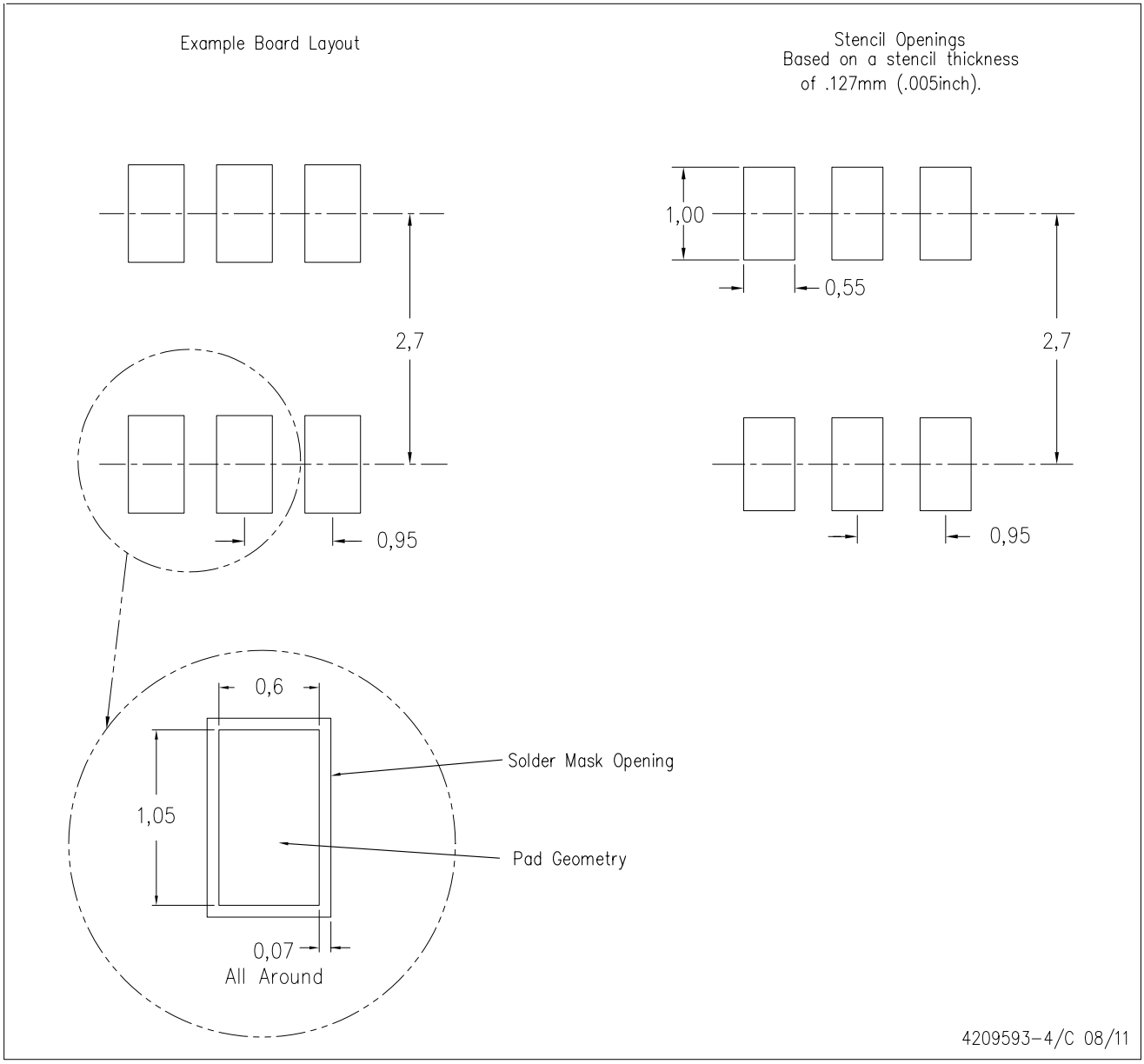
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2S017DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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